WBS 6.6.1.1 & 6.6.3.2
Muon TDC and Mezzanine Cards
Technical Overview

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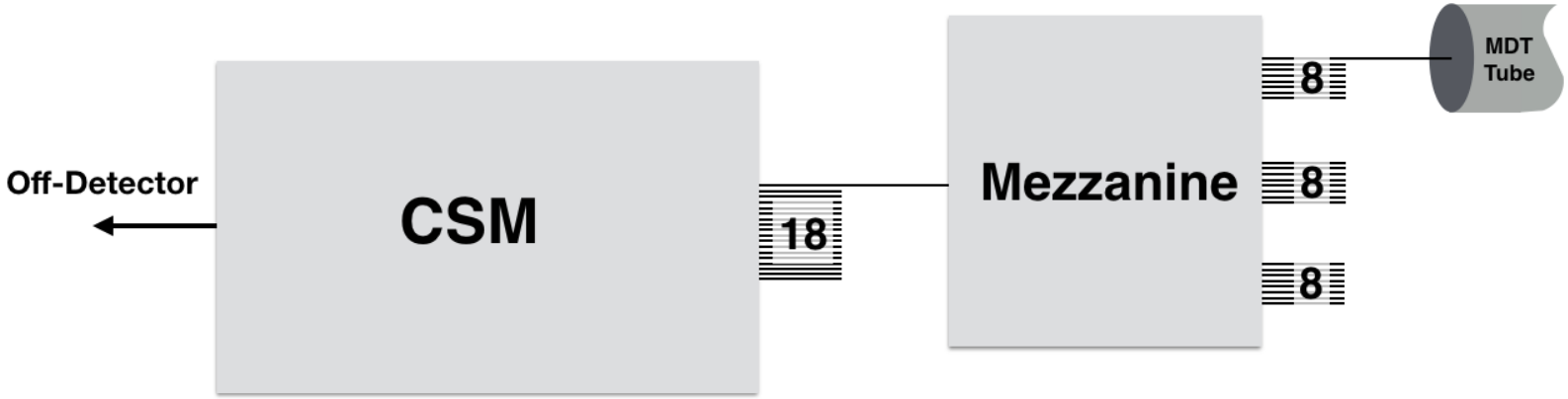
Group Expertise

- Elliott Cheu
  - Professor of Physics, University of Arizona
  - Member of ATLAS since 2005
  - Developed electronic calibration system for CSC
  - Oversees electronics group including two electrical engineers
- Arizona
  - Cathode Strip Chamber (CSC) pulser system
  - Phase-I Upgrade: Developing front end boards for New Small Wheel Micromegas chambers
    - Mini-1 test cards
    - MMFE-8 demonstrator boards
    - ~5,000 boards

Group Expertise

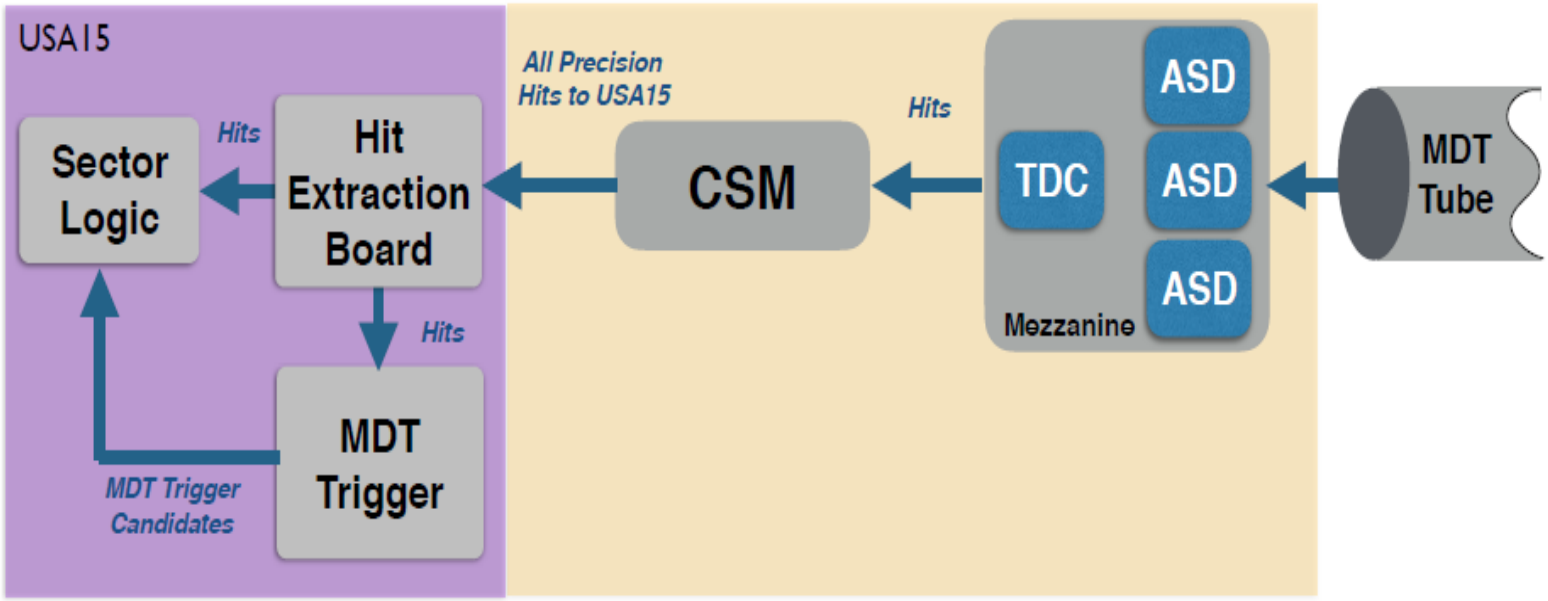
- Michigan
  - Designed three ASICs for previous collider experiments;
  - Designing the trigger data serializer (TDS) chip for the ATLAS Phase-I NSW upgrade
    - Uses the GlobalFoundries 130 nm technology
    - More complicated than the HL-LHC TDC chip
  - Proposed and have been intensively studying trigger-less mode with simulations and with the current MDT setup
  - Have played an important role in the current MDT frontend electronics commissioning
    - Discovered a few design problems with the current ASD and AMT chips.
  - Currently responsible for the daily operation of the whole ATLAS MDT system including electronics, gas and calibration

Current Muon Readout System



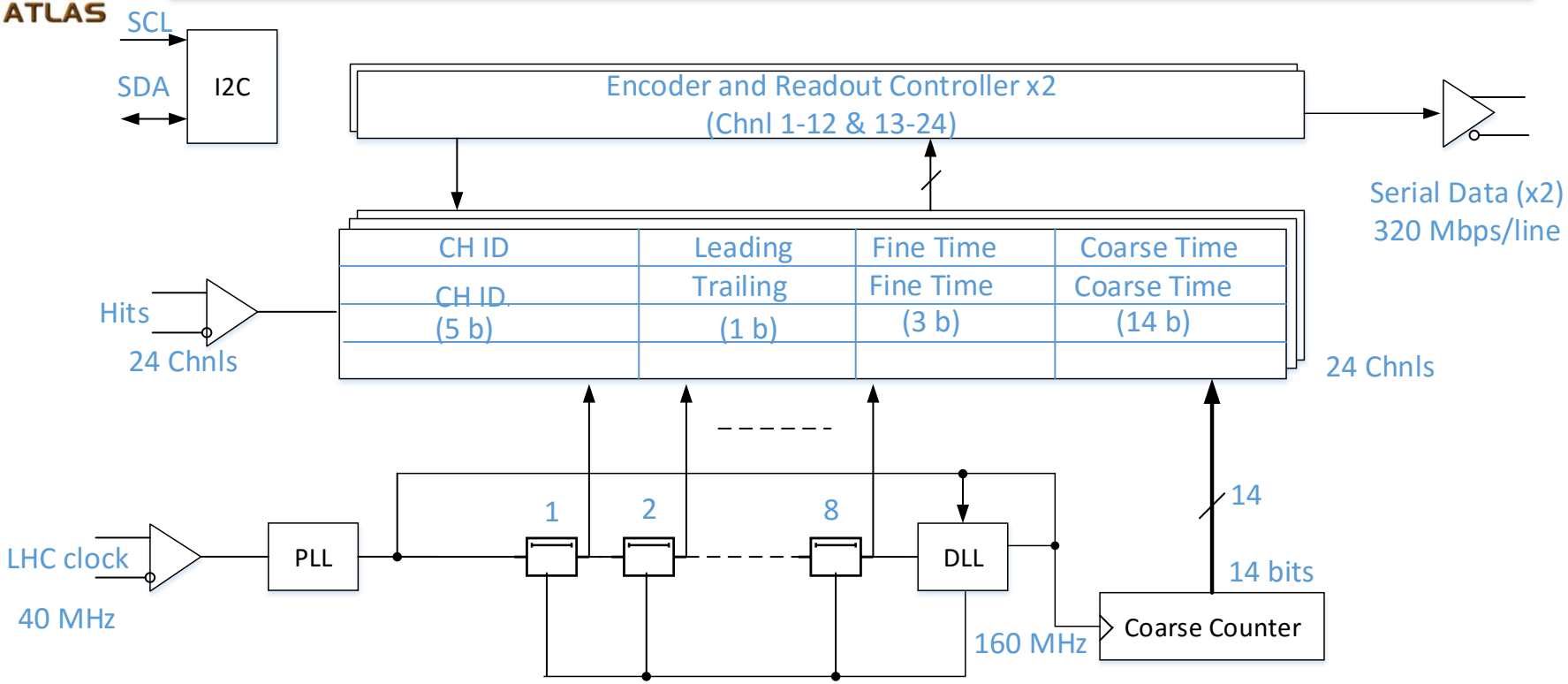
- Expect MDT rate to be 300 kHz/tube in HL-LHC era
- Expected output from each Mezzanine card will be 260 Mbps
- Current cards can handle 80 Mbps
- Currently MDTs do not participate in L0 trigger

HL-LHC Muon Readout System



- New TDC ASIC designed to handle rate
- Michigan will design, prototype, fabricate and test 22,000 time-to-digital converter (TDC) ASICs for the HL-LHC upgrade
  - Takes into account die fabrication and chip packaging
- Arizona will design, prototype, fabricate and test 17,225 Mezzanine cards for the HL-LHC upgrade

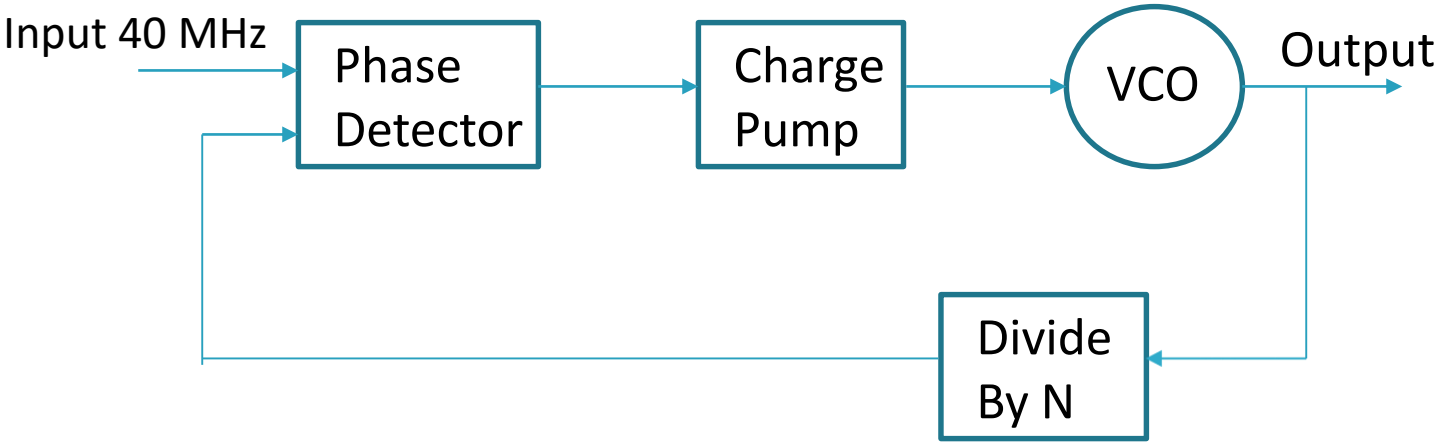
Proposed TDC



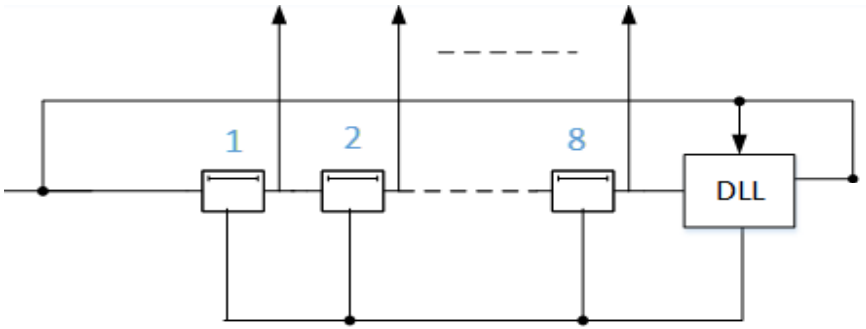
- Each TDC handles 24 channels with a timing resolution of 0.78 ns
- Phase-locked loop (PLL) and Delay-locked loop (DLL) need custom-layout
- Other logic parts are standard-cell designs (high-level design with Verilog and later converted into silicon using the Cadence tool)

PLL and DLL

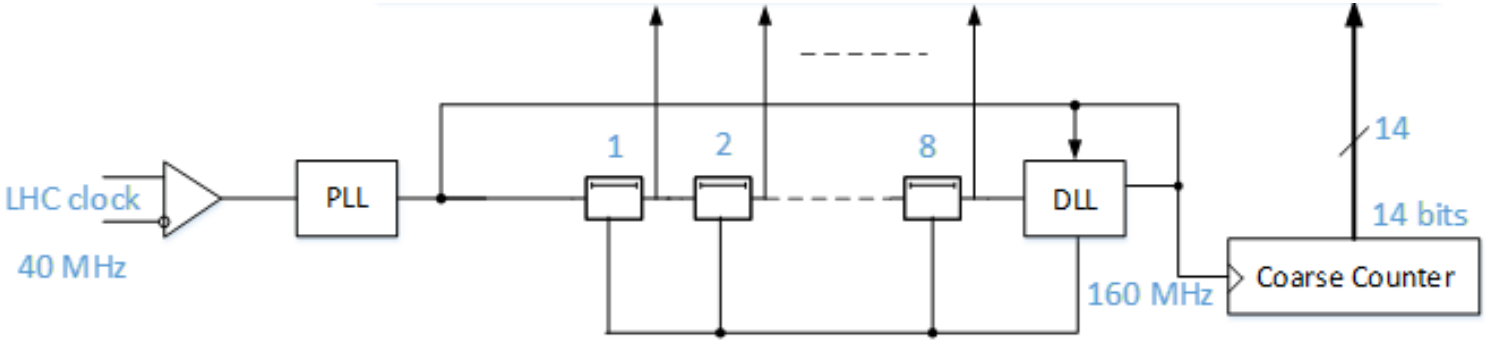
- PLL: reduces the input clock jitter, and performs frequency multiplication (input 40 MHz → output 40, 80, 160, 320 MHz)
  - Negative feedback loop, use phase detector to detect the phase difference of input and output clocks and VCO to adjust the phase



- DLL: similar to PLL but only delays input clock (delay step size: clock period divided by number of delay cells)



TDC Timing Measurement



- TDC timing resolution of 0.78 ns is achieved
  - The internal clock is running at 160 MHz → 12 bit BCID + 2 sub-BCID bits (coarse counter) to obtain a timing resolution of 6.25 ns
  - 8 delay cells (3 bits fine counter) to obtain a timing resolution of 6.25/8=0.78 ns
  - Similar to Hour (BCID – 25 ns): minute (sub-BCID – 6.25 ns): second (fine time – 0.78 ns)

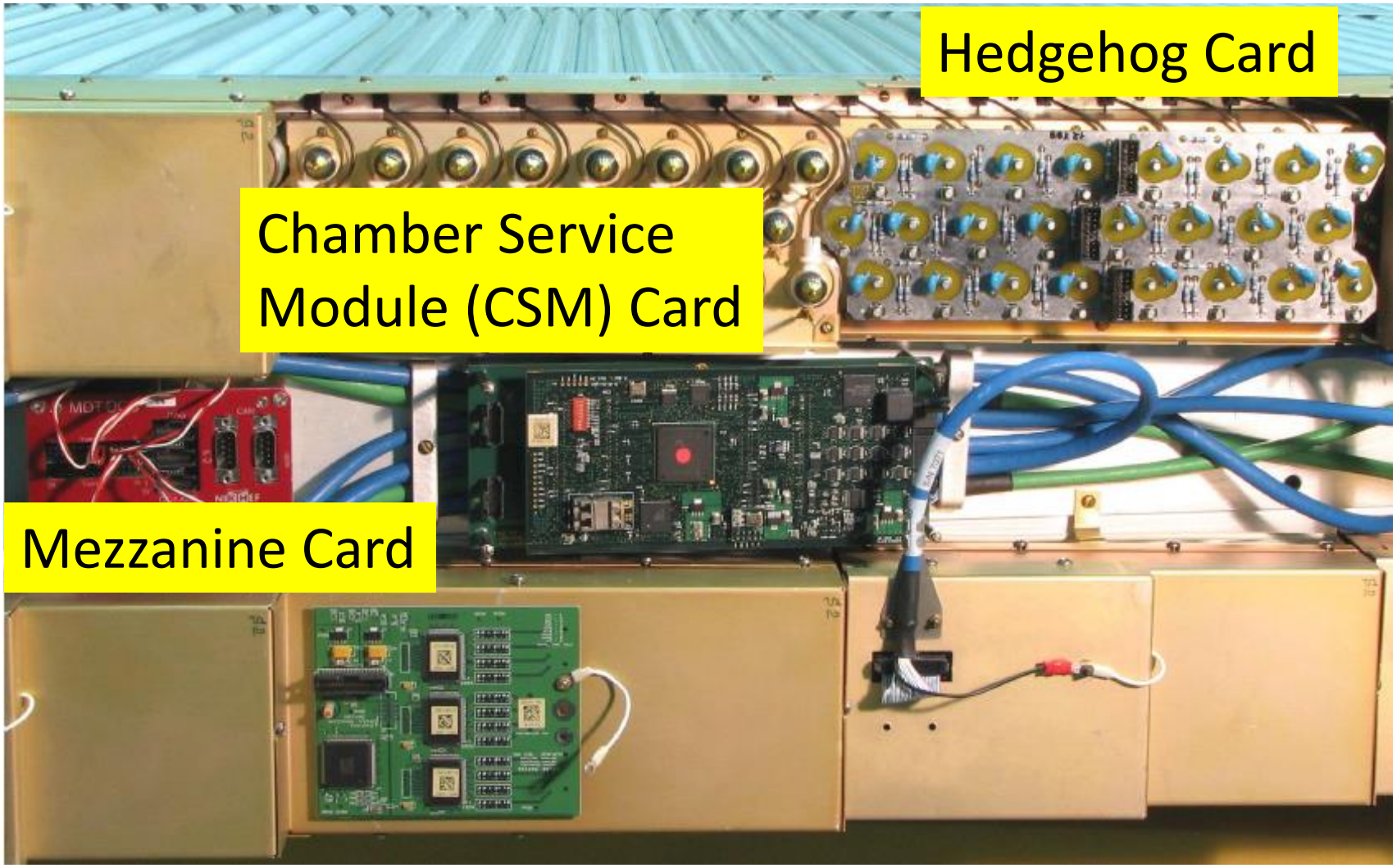
TDC Design

- Two prototype runs ($100k per run with 40 chips produced)
- One pre-production run (~2k chips) followed by final production run ($477k with ~20k chips produced)
- For each run, we need to:
  - Design, fabricate substrates, and assemble ASIC packaging ($176k for packaging 22k chips)
  - Build chip test fixture (often PCB+FPGA+TDC) ($10k per chip test fixture)
  - Test produced chips in different conditions to figure out possible design problems and fix bugs found
- Final chip testing:
  - At least two test fixtures needed to speed up the testing process
  - Use test sockets on PCB for chip production testing
  - Estimate 30 minutes to test each ASIC and three times as long to test a problematic ASIC
  - Test results are recorded in a database

Mezzanine Card

- Inputs
  - Analog signals from 24 MDT tubes
  - Trigger, timing and control information
- Outputs
  - 2 x serial out at 320 Mbps of hit address and leading and trailing precision times
- Functionality
  - Amplifies, shapes and discriminates raw TDC pulses (via ASIC)
  - Digitization of the arrival time of the leading and trailing signal edges (via ASIC)
  - Appropriate buffer depth (via ASIC)
  - ASIC protection from overvoltage or tube discharge conditions

Mezzanine Card



Mezzanine Card Design

- Demonstrator board including CSM simulator
- Two prototype runs
- One pre-production run (1722 boards)
- Followed by final production run (15,502 boards)
- Each design cycle is tied to a run of the TDC ASICs
- Final board testing:
  - At least two test fixtures needed to speed up the testing process
  - Use test sockets on PCB for chip production testing
  - Estimate 15 minutes to test each board and two times as long to test a problematic board
  - Test results are recorded in a database

TDC R&D

- MDT hit data rates studies and definition of TDC specifications
- Custom-layout design and simulation for PLL and DLL
- Standard-cell design and simulation for other logic parts and also configuration and monitoring
- Floorplan, layout and fabrication of the 1st prototype
- Package design for the 1st prototype

Mezzanine Board R&D

- Demonstrator boards
  - Proof of concept using FPGA to simulate TDC
- CSM simulator
  - To receive outputs from Mezzanine cards
- MDT simulator
  - Pulser to provide simulated inputs to ASD ASICs
- Test rigs
  - Test operation of Mezzanine cards

TDC ASIC Schedule

- FY19: 1st prototype run
- FY20: 2nd prototype run
- FY21: Pre-production run
- FY22: Final production run
- FY23: Production chip testing

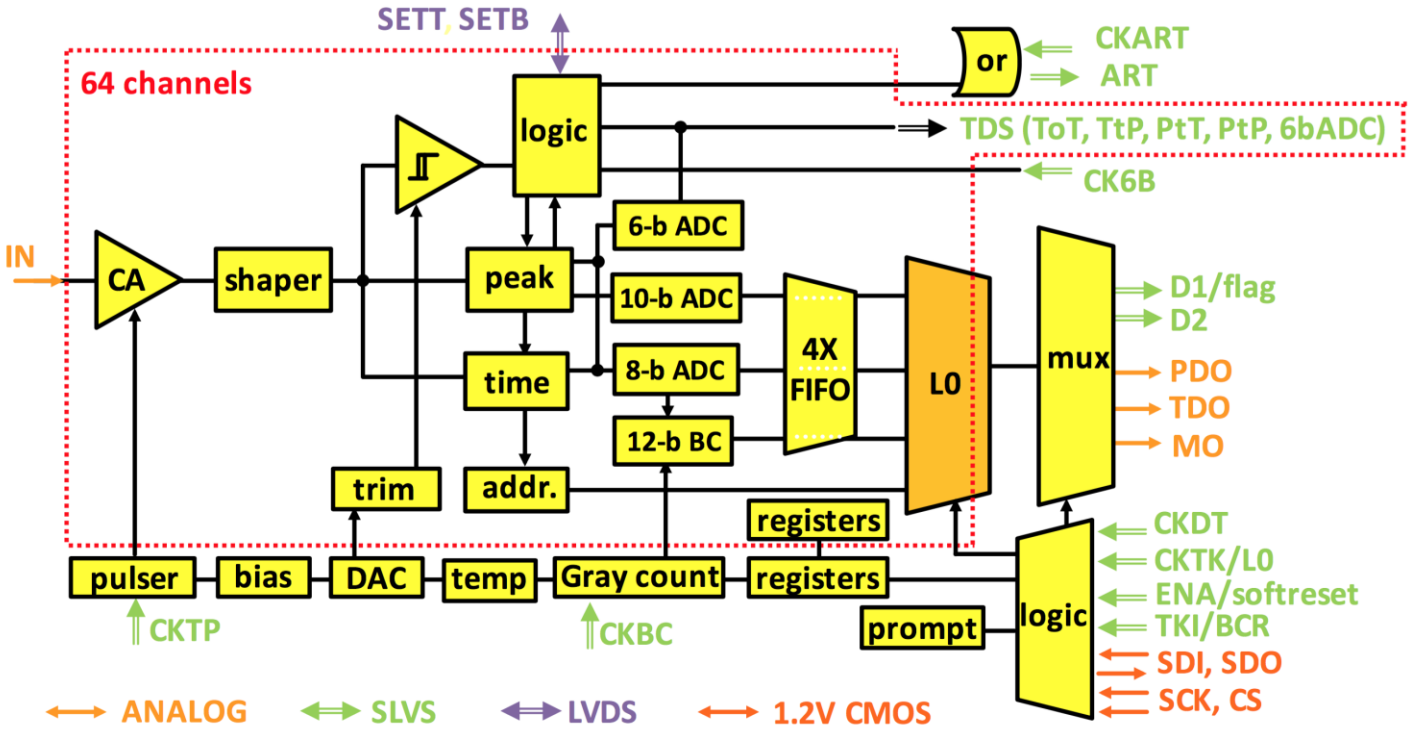
- Pre-production run should provide enough chips for the urgent need of testing sMDT chambers
- Tested chips will be shipped to the mezzanine card production site every month

Mezzanine Card Schedule

- FY17-FY19: Design, build and test demonstrator board
- FY20: Pre-prototype mezzanine board
- FY21: Prototype boards
- FY22: Design and build pre-production boards
- FY23: Build and test production boards

- Mezzanine card schedule tied to Michigan TDC ASIC production

VMM Solution



- VMM ASIC designed for readout of New Small Wheel
- ASD and TDC functionality combined in a single chip
- Minor modifications would allow this chip to be used for HL-LHC
  - Decision will be made around time of Muon TDR

TDC Estimated Cost

- Based on past experience with the TDS design and actual quotes from companies
- Total estimated cost: $1593.5k
- Manpower cost $770.5k in total:
  - 1.7 engineer for the TDC design and packaging, 2.8 engineer assistants to design test fixtures and develop firmware, 4 students for chip testing
- Material cost $805k in total:
  - $100k for the second prototype run and packaging (1st prototype from R&D)
  - $477k for final production ($405k non-recurring engineering cost, and $72k for 20 wafers with $3.6k per wafer to produce all 22k TDCs)
  - $176k for packaging ($8x22k)
  - $10k for setting up the chip test fixture for the second prototype run (1st prototype from R&D, mainly used to pay PCB+assembly+FPGA)
  - $20k for setting up several chip test fixtures for the production run
  - $20k for cadence software license
- Travel cost: $18k in total:
  - 4 trips to CERN for discussions on TDC and testing ($3k per trip)
  - 1 trip to international conference to show the TDC design
  - 1 trip to the packaging company to discuss on final chip packaging

Mezzanine Card Estimated Cost

- Total estimated cost: $2,046K
- Manpower cost $706K in total:
  - 2.0 engineer for design and development, 2.0 engineer assistants to design software and firmware, 4.2 students for board testing
- Material cost $1,318K in total:
  - $90K Design
  - $128K Prototype
  - $1,099K Production and Testing
- Travel cost: $21.8K in total:
  - 4 domestic trips (collaboration on TDC and CSM)
  - 4 international trips to CERN (prototyping and production)

Costs and Risks

- Risk methodology
  - TDC
    - Most complex designs have been implemented before
    - Schedule risk can be mitigated through parallel testing
  - Mezzanine
    - Much of risk assumed tied to ASIC availability and design
    - Schedule risk includes a factor of two
- Cost methodology
  - TDC
    - Based upon TDS submission
      - Same process
      - More complex
  - Mezzanine
    - Parts from previous mezzanine board
    - Board costs from Phase I prototypes
    - Scaling based upon Phase I prototypes